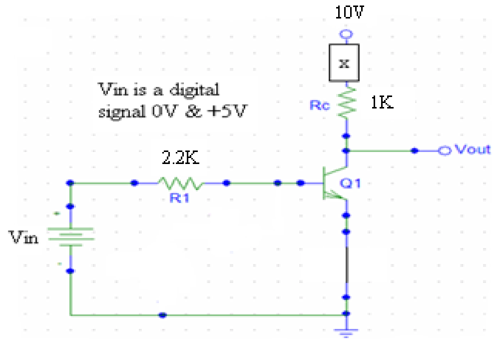
ELECTRICAL ENGINEERING DEPARTMENT

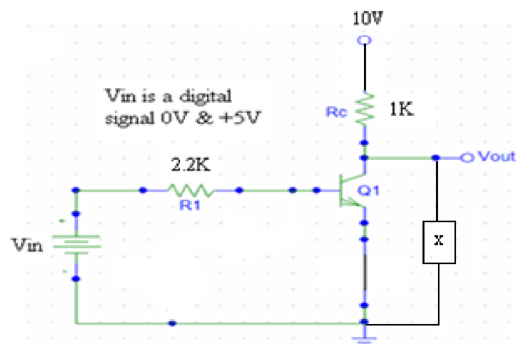
California Polytechnic State University

EE 361	BJT Common-Emitter Switch & Digital to Analog Converter (DAC)	Pre-lab 6

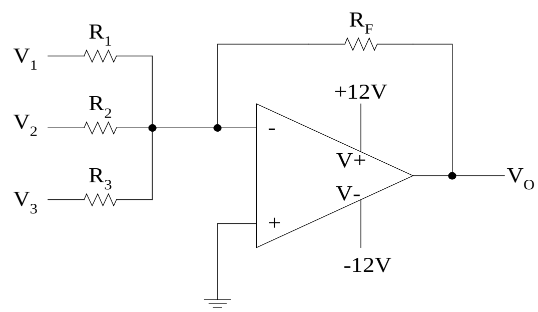
1. For the ideal BJT common-emitter switch circuit, determine the value of V_{in} for which the device x operates. In addition, calculate V_{out} and i_{RC} if device x is an LED with V_{FB} = 2V. Also, determine i_{R1} when LED is lit. BJT, Q1, is made of silicon.



2. Repeat #1 for BJT switch circuit below.



3. For the summing amplifier, <u>derive</u> V_o with $R_2 = 2R_1$, $R_3 = 2R_2$ and $R_F = R_3$.
   Also, if input voltages V_1, V_2 and V_3 are digital signals (bits) with only two possible values, 0V or -1V (minus one volt), calculate all possible V_o values.
   Hint: There are eight possible V_o values.



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Objective

Investigate the use of a BJT as a switch and the operation of a summing amplifier as a DAC.

Workbench Equipment

- Digital Oscilloscope, Keysight InfiniiVision MSO-X2022A
- Function Generator, Agilent 33120A or Agilent 33220A
- Digital Multimeter, Agilent 34401A
- DC Power Supply, Agilent E3640A
- Dual-tracking DC Power Supply, TPS-4000

Check-out Equipment, 20-111 window

- Scope Probe (10:1), 2
- Banana to grabber 3 pair, 3red / 3black
- Banana to Banana lead, 3
- BNC to grabber lead

Background

BJT Common-Emitter Switch Analysis

As seen in experiment #3 a BJT can be used in a circuit to amplify a signal. A BJT can also be used in a circuit as a switch (see Figure 6-1), as will be demonstrated in this experiment.

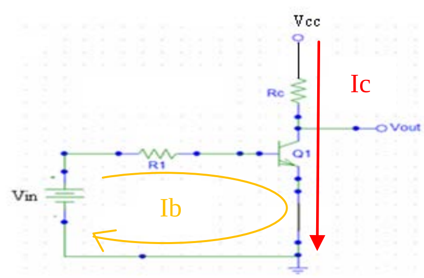


Fig. 6-1 BJT Switch Circuit

To operate a BJT as a switch requires two important conditions. One, V_{in} is a digital signal where one voltage value of V_{in} (usually 0V) reverse biases the base-emitter junction and the other V_{in} voltage value (often +5V) forward biases the base-emitter. Second, the value of the base resistor, R1, is selected as to make V_{CE} = 0V when V_{in} = +5V. In other words, under these two conditions, the BJT is operated in either the cut-off region or saturation region of its I_C v. V_{CE} plot (Figure 6-2).

When V_{in} = 0V, base current ideally equals zero (actually very small) and therefore collector current ideally equals zero (also actually very small) and the BJT is in cut-off. When V_{in} = +5V, base and collector currents flow and V_{CE} = 0V since ideally all the source voltage, V_{CC}, is dropped across R_C due to the design value of R1. In actuality there is a small V_{CE} usually a couple tenths of volts. Thereby the BJT is saturated since V_{CE} is small and there's current gain, ß. Although, current gain is not optimum, $ß \neq ß_{spec}$, since BJT not operated in the active region.

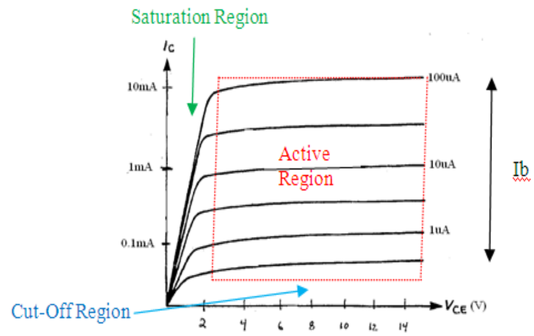


Fig. 6-2 I_C v. V_{CE}

To calculate base current, KVL around base loop yields: $$I_b = \frac{V_{in} - V_{FB}}{R_1} \qquad (6\text{-}1)$$

Where $I_b = 0$ ideally when $V_{in} = 0V$

To calculate collector current, $I_C \neq ß_{spec}Ib$ since BJT switch is not operated in active region.

By KVL: $$I_C = \frac{V_{cc}}{R_C} \qquad (6\text{-}2)$$

Where $I_C = 0$ ideally when $I_b = 0$

If a device, such as a LED, is added into collector loop, equation 6-2 is modified to account for voltage across device.

Procedure 1: BJT Switch

- Build circuit of prelab #1. Use red LED as device x, use Agilent E3640A power supply for V_{in} set initially to 0V and use TPS4000 power supply for V_{cc} = 10V.
    - o Recall (experiment #3) how to determine emitter, base and collector leads of BJT, if not, consult instructor.
- Measure voltage across R_1 and Rc and calculate I_b and I_C.

  V_{R1} = ______________ V_{RC} = _______________ I_b = ______________ I_C = ______________
- Repeat previous step for V_{in} = +5V.

  V_{R1} = ______________ V_{RC} = _______________ I_b = ______________ I_C = ______________

- Calculate current gain ß and compare to ßspec. ß = ______________
- Before proceeding, have instructor verify LED lights for V_{in} = +5V and LED does not light for V_{in} = 0V.

  Instructor Initials: _________

- Change circuit to that of prelab #2 by relocating red LED in circuit and set V_{in} = +5V.
- Measure voltage across R_1 and Rc and calculate I_b and I_C.

V_{R1} = ____________ V_{RC} = _____________ I_b = ____________ I_C = ____________

- Repeat previous step for V_{in} = 0V.

  V_{R1} = ____________ V_{RC} = _____________ I_b = ____________ I_C = ____________

- Before proceeding, have instructor verify LED lights for V_{in} = 0V and LED does not light for V_{in} = +5V.

  Instructor Initials: ________

Procedure 2: DAC (Digital-to-Analog Converter)

- Build the circuit of Figure 6-3. Inside the diagram box is a summing amplifier. Outside box is a 74163 IC, a binary counter which provides digital inputs to the summing amplifier. Pin diagram and basic operation of 74163 follows Discussion section of this experiment.
  - o Highly Recommended: Build summing amplifier and counter IC circuits separately and test separately before connecting together.
  - o To test summing amplifier separately, connect all four inputs to 3.5 V DC and measure Vo with DVM and compare against theoretical Vo.
  - o To test counter IC separately, connect pin 1 to +5V (disables Clear) and connect a 0V to 5V 1KHz square wave signal to pin2 (Clock). Use Scope to verify Q outputs have square waves 0V to approximately 4V at ($\frac{1}{2}, \frac{1}{4}, \frac{1}{8}, \frac{1}{16}$) times the clock frequency.

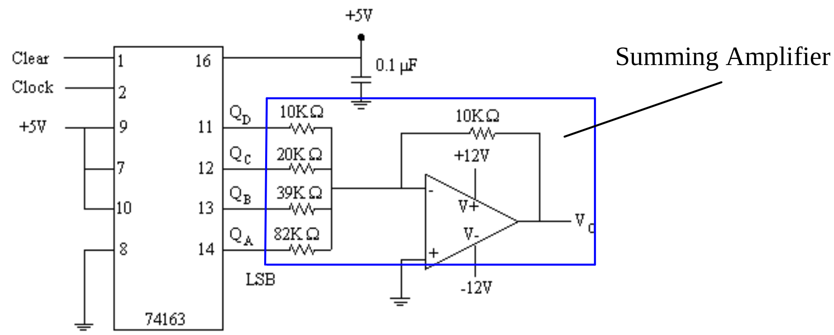


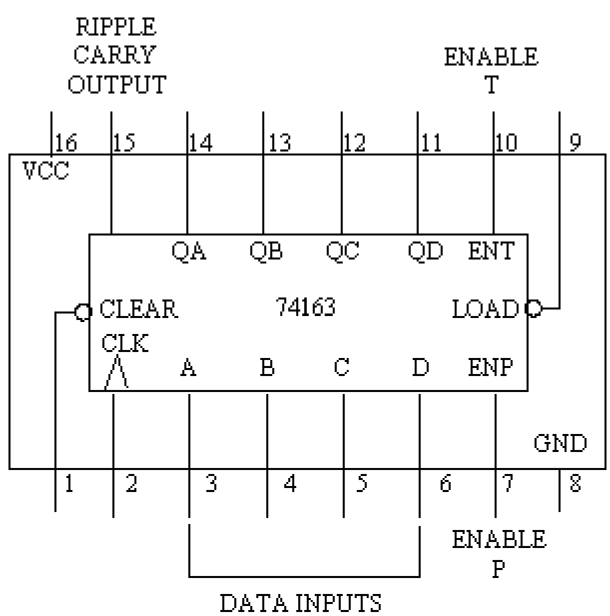
Fig. 6-3 DAC Circuit

- Calculate V_o for all possible input values (use 0V for '0' and use +3.5V for '1') and record in Table 6-3.
- **<u>Momentarily</u>** ground Clear input of 74163 to ensure summing amplifier inputs start at 0000.
- Use function generator (Hi Z mode) to apply a 0V to 5V **1Hz** square wave signal at the 74163 Clock input.
  - o Observe square wave on scope and make certain square wave does not go below zero volts (ground). Adjust DC offset of function generator if below ground.
- Measure V_o with DVM for each binary count 0000 -> 1111 and record in Table 6-3.
  - o May need to temporarily disconnect 1Hz clock to make V_o measurement.

- Use function generator (Hi Z mode) to apply a 0V to 5V **1KHz** square wave signal at the 74163 Clock input.
    - o Observe square wave on scope and make certain square wave does not go below zero volts (ground).
- Observe V_o with scope. Capture staircase-like waveform.

Count	$V_{o\ TH}$ (V)	$V_{o\ EXP}$ (V)
0000		
0001		
0010		
0011		
0100		
0101		
0110		
0111		
1000		
1001		
1010		
1011		
1100		
1101		
1110		
1111		

Table 6-3 DAC Data



74163 Pin Diagram:

74163 Basic Operation:

The 74163 IC counts in binary from 0000 to 1111 (zero to fifteen), the count is at outputs QA through QD where QA is the LSB (Least Significant Bit) = furthest to the right bit of binary number. When a positive to negative transition voltage is connected to the CLK input and the CLEAR input is connected to +5V, the outputs will increment one in binary. For example, if outputs equal 1011 (eleven) before positive to negative transition is applied, outputs equal 1100 (twelve) after positive to negative transition occurs. If the CLEAR input is connected to ground, outputs QD through QA will equal zero regardless what the CLK input equals.

Discussion

1. How does your comparison of calculated ß to $ß_{spec}$ in procedure 1 prove the BJT operates in the saturation region?
2. Explain why the LED does not light when V_{in} = +5V for the circuit of prelab #2.
3. Explain how a linear ramp function can be obtained by smoothing out the staircase waveform output of the digital-to-analog converter (DAC).